UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,546	12/27/2001	Fong-Long Lin	2102397-992070	7492

26379 7590 11/14/2003

GRAY CARY WARE & FREIDENRICH LLP
2000 UNIVERSITY AVENUE
E. PALO ALTO, CA 94303-2248

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,546	LIN ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- Th MAILING DATE of this communication appears on the cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/ Declaration

1. The oath/declaration filed on 12/27/01 is acceptable.

Drawings

2. The drawings filed on 12/27/01 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

A. The claim limitations as recited in the claim 11, lines 14 and 15, include "said first chip to be coupled to an in-circuit emulator".

B. The claim limitation as recited in the claim 12, line 3, includes "said in-circuit emulator".

Therefore, the "in-circuit emulator" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

4. If applicant is aware of any relevant prior art, he/she requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 5-7, 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Reddy (US Pat. 6403448).

Regarding claim 1, Reddy discloses a double die/double chip device/bond out chip (10 in Fig. 2a/2b; 10a/10b in Fig. 3) having a chip-to-chip/bond out configuration, the double chip/bond out chip comprising:

- a first chip/device (10a in Fig. 3, also shown as one of the double die/chip 10 in Fig. 2a/2b; Col. 4, lines 24-31)

- a second chip/device (10b in Fig. 3, also shown as another one of the double die/chip 10 in Fig. 2a/2b; Col. 4, lines 24-31)
- a plurality of input/output (I/O) pads (76 in Fig. 4; Col. 6, line 67) and buffer pads (38 in Fig. 4; Col. 4, line 67; Col. 5, lines 15-20) being disposed on the first and second chips/devices, the second chip/device being adjacent to the first chip/device and being electrically/communicatively coupled to the first chip/device (Col. 4, lines 31-36), and
- the first and second chips/devices being spaced apart from each other (see 10 in Fig. 2a/2b and 10a/10b in Fig. 3), being separated by a scribe line (see 16 in Fig. 2a; Col. 4, lines 1-6) and being formed on a semiconductor wafer (12 in Fig. 2a and 2b; Col. 3, line 65)

(Fig. 1a-6a and 7; Col. 3, line 62- Col. 6, line 15).

Regarding claim 2, Reddy teaches substantially the entire claimed structure as applied to claim 1 above, wherein Reddy teaches the first chip/device and the second chip/device being spaced apart (see 10 in Fig. 2a/2b and 10a/10b in Fig. 3) and being separated by the scribe line (see 16 in Fig. 2a; Col. 4, lines 1-6).

Regarding claim 3, Reddy teaches substantially the entire claimed structure as applied to claim 1 above, wherein Reddy further teaches the first and second chips/devices being substantially identical in architecture/fabrication processing to a

production/conventional chip (see 4 in Fig. 1a-1c; Col. 3, lines 45-62) with an exception of an interconnect scheme/connection layer comprising interconnect lines/members (14/32/34/36 in Fig. 2a/2b-4; 52/54/58 in Fig. 4/6a; Col. 3, line 66- Col. 4, line 4; Col. 4, line 10; Col. 4, lines 31-35; Col. 5, line 40- Col. 6, line 3).

Regarding claim 5, Reddy teaches substantially the entire claimed structure as applied to claims 1, 3 and 4 above, wherein Reddy teaches the first and second chips/devices being formed on the semiconductor wafer (12 in Fig. 2a and 2b; Col. 3, line 65).

Regarding claim 6, Reddy teaches substantially the entire claimed structure as applied to claims 1 and 3-5 above, wherein Reddy further teaches the wafer having a plurality of fields/reticle zones (not numerically referenced in Fig. 2a/2b-see 2 in Fig. 1b) where a plurality of chips/devices are typically fabricated (Col. 3, lines 51-53 and 63-66), the fields/reticle zones including two or more chips/devices (see the devices 4 in the zones 2 in Fig. 1b).

Regarding claim 7, Reddy teaches substantially the entire claimed structure as applied to claims 1 and 2 above, wherein Reddy further teaches the first chip/device and the second chip/device including an active core/memory portion (not numerically referenced- see 8 memory blocks in 10a or 10b in Fig. 4; Col. 4, lines 55-65) and one of the first and second chips/devices or both chips/devices being functional/operated in a

single mode or double device mode configuration respectively as predetermined/controlled by a mode signal from the mode circuit (Col. 3, line 66- Col. 4, line 9). The single mode configuration being achieved by disabling the interconnect lines/layers (32/34/36 and 42/48 in Fig. 3 and 4 respectively; 50/54/58 in Fig. 4, 5 and 6a) connected to the active core/memory portion of the one of the chips/devices such that the respective active core/memory portion becomes inactive/disabled (Col. 4, lines 45-50; Col. 5, lines 7-20; Col. 6, lines 40-65).

Regarding claim 9, Reddy teaches substantially the entire claimed structure as applied to claim 1 above, wherein Reddy further teaches a buffer circuit being electrically/communicatively coupled to the plurality of respective pads/I/O buffer pads (38 in Fig. 4; Col. 4, line 67; individual I/O signal paths not referenced in Fig. 4; Col. 5, lines 15-20) on the first and the second chips/device respectively.

Regarding claim 10, Reddy teaches substantially the entire claimed structure as applied to claim 1 above, wherein Reddy further teaches the first and second chips/devices having memory devices comprising a variety of circuit configurations including those being functional as control/microcontroller circuits (28 and 46a/46b in Fig. 3 and 4 respectively; Col. 4, lines 25-28; Col. 5, lines 1-30).

Claim Rej ctions - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4, 8 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy (US Pat. 6403448).

Regarding claim 4, Reddy teaches substantially the entire claimed structure as applied to claim 1 above, except the second chip being substantially identical in architecture to the first chip with an exception of a connection layer.

Reddy further teaches in another embodiment of Fig. 6c, the interconnect structure where the conductor areas are formed in the substrate (Col. 6, lines 25-30) instead of those in the first chip/device having the first conductive layer (see configuration of 52 in Fig. 6a and 6c).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second chip being substantially identical in architecture to the first chip with an exception of a connection layer as taught by the

embodiment of Fig. 6c in so that the number of metallization layers can be reduced and photolithography processing can be simplified in Reddy's bond out chip.

Regarding claim 8, Reddy teaches substantially the entire claimed structure as applied to claims 1, 2 and 7 above, wherein Reddy further teaches the active and inactive/disabled core portions being formed in one of the two chips/devices by using the respective interconnect lines/connection layer (42/48 in Fig. 4 and 32/34/36 in Fig. 3) in the double device or single device mode configuration connected to the active core/memory portion of the one of the chips/devices (Col. 4, lines 45-50; Col. 5, lines 7-20; Col. 6, lines 40-65). Reddy further teaches an interconnection layer/second conductive layer (54 in Fig. 5 and 6a; Col. 5, line 55) being disposed above the connection layer/first conductive layer (52 in Fig. 6a; Col. 5, line 58) such that the interconnection layer/second conductive layer traverses the scribe line and electrically/communicatively couples the I/O pads of the first or second chip/device (see partial views in Fig. 5 and 6a; Col. 5, line 42- Col. 6, line 15).

Regarding claim 8, the claim limitations "the disabled core portion is disabled by use of a at least one connection layer and said active core portion is activated by use of said at least one connection layer" do not distinguish over Reddy, because only the final product/structure is relevant, not the process of making such as "using the connection layer" or "etching, laser stripping or disconnecting a connection layer". Note that a

"product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 11, Reddy discloses a double die/double chip device/bond out chip (10 in Fig. 2a/2b; 10a/10b in Fig. 3) having a chip-to-chip/bond out configuration, being formed on the semiconductor wafer (12 in Fig. 2a and 2b; Col. 3, line 65), the double chip/bond out chip comprising:

- a first chip/device (10a in Fig. 3, also shown as one of the double die/chip 10 in Fig. 2a/2b; Col. 4, lines 24-31)
- an adjacent/second chip/device (10b in Fig. 3, also shown as another one of the double die/chip 10 in Fig. 2a/2b; Col. 4, lines 24-31)
- the first and second chips/devices being substantially identical in architecture/fabrication processing to a production/conventional chip (see 4 in

Fig. 1a-1c; Col. 3, lines 45-62) with an exception of an interconnect scheme/connection layer comprising interconnect lines/members (14/32/34/36 in Fig. 2a/2b-4; 52/54/58 in Fig. 4/6a; Col. 3, line 66- Col. 4, line 4; Col. 4, line 10; Col. 4, lines 31-35; Col. 5, line 40- Col. 6, line 3).

- the first chip/device and the adjacent/second chip/device being spaced apart (see 10 in Fig. 2a/2b and 10a/10b in Fig. 3) and being separated by the scribe line (see 16 in Fig. 2a; Col. 4, lines 1-6), and
- a plurality of I/O buffers (38 in Fig. 4; Col. 4, line 67; Col. 5, lines 15-20) and pads (76 in Fig. 4; Col. 6, line 67) being disposed on the first and second chips/devices, the adjacent/second chip/device being electrically/communicatively coupled to the first chip/device (Col. 4, lines 31-36), (Fig. 1a-6a and 7; Col. 3, line 62- Col. 6, line 15).

Reddy further teaches the first chip/device and the adjacent/second chip/device including an active core/memory portion (not numerically referenced- see 8 memory blocks in 10a or 10b in Fig. 4; Col. 4, lines 55-65) and one of the first and second chips/devices or both chips/devices being functional/operated in a single mode or double device mode configuration respectively as predetermined/controlled by a mode signal from the mode circuit/emulator circuit (Col. 3, line 66- Col. 4, line 9). Such configuration being capable of providing the desired circuit paths to any of the I/O, buffer or memory core portions across the scribe lines

through the timing, driver, decoder and control signals controlled by the mode circuit/emulator circuit (Col. 5, lines 1-30).

Reddy fails to teach the second chip being substantially identical in architecture to the first chip with an exception of a connection layer.

Reddy further teaches in another embodiment of Fig. 6c, the interconnect structure where the conductor areas are formed in the substrate (Col. 6, lines 25-30) instead of those in the first chip/device having the first conductive layer (see configuration of 52 in Fig. 6a and 6c).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second chip being substantially identical in architecture to the first chip with an exception of the connection layer as taught by Reddy in the embodiment of Fig. 6c so that the number of metallization layers can be reduced and photolithography processing can be simplified in Reddy's bond out chip.

Regarding claim 12, Reddy teaches substantially the entire claimed structure as applied to claim 11 above, wherein Reddy further teaches the mode circuit/emulator circuit (30 in Fig. 4) being electrically/communicatively coupled to the plurality of respective I/O pads, buffer pads and drivers (38, 76 and 74 respectively in Fig. 4 and 7; Col. 5, lines 1-30; Col. 6, lines 39-46).

Regarding claim 13, Reddy teaches substantially the entire claimed structure as applied to claims 11 and 12 above, wherein Reddy further teaches the double chip/bond out chip comprising interconnect lines/connection layer/connection members (42/48 in Fig. 4 and 7; 52 in Fig. 6a; Col. 6, lines 39-65; Col. 4, line 65- Col. 6, line 3 for electrically/communicatively coupling/activating the desired I/O pads, buffers and drivers (76/38 in Fig. 4 and 74 in Fig. 7 respectively) to the respective first and the adjacent/second chip/devices.

Regarding claim 14, Reddy teaches substantially the entire claimed structure as applied to claims 11-13 above, wherein Reddy further teaches the first and adjacent/second chips/devices having the memory devices comprising the variety of circuit configurations including those being functional as control/microcontroller circuits (28 and 46a/46b in Fig. 3 and 4 respectively; Col. 4, lines 25-28; Col. 5, lines 1-30).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B and C are cited as being related to chip arrays having mutichip interconnect structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

Nitin Parekh

PATENT EAMINER

TECHNOLOGY CENTER 2800

NP

11-06-03